# METHOD AND APPARATUS FOR UNIVERSAL PROGRAM CONTROLLED BUS ARCHITECTURE

## REFERENCE TO RELATED APPLICATION

This application is a continuation of U.S. Application No. 10/412,975 filed April 11, 2003, which is a continuation of U.S. Application No. 10/231,320 filed August 28, 2002, U.S. Patent No. 6,624,658, which is a continuation of U.S. Application No. 09/960,916 filed September 24, 2001, U.S. Patent No. 6,504,399, which is a continuation of U.S. Application No. 09/243,998 filed February 4, 1999, U.S. Patent No. 6,329,839, which is a continuation of U.S. Application No. 08/708,403 filed September 4, 1996, U.S. Patent No. 6,034,547.

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## BACKGROUND OF THE INVENTION

### 1. FIELD OF THE INVENTION

The present invention is directed to a programmable, configurable bus system of liens to interconnect electrical components for an electrical/electronics system.

### 2. ART BACKGROUND

Megacells are described as block components such as static random access memory (SRAM), microcontrollers, microprocessors and buffers. Sometimes it is desirable to interconnect a plurality of megacells together to provide a larger functional entity. One way to interconnect multiple megacells and logic circuits is through a hardwired bus system. Examples are illustrated in **Figures 1a, 1b** and **1c. Figure 1a** illustrates a bus interface to a dual port SRAM megacell. Bus lines include DATA 0 - DATA15, READA0 - READA9, WRITEA0 - WRITEA9. To couple multiple megacells, the data lines are shared among the coupled cells. However, separate read and write lines would be required for each megacell. To the contrary, if the megacells were coupled to